IN THE CLAIMS

1. (Currently Amended) In a programmable logic device (PLD) having a JTAG port, a decryptor for decrypting an encrypted bitstream, and a memory for storing decryption keys used by the decryptor to decrypt the encrypted bitstream, a method for loading the keys comprising:

placing the PLD into a printed circuit board;

testing the printed circuit board using the JTAG port of the PLD; and

loading the decryption keys into the memory using the JTAG port.

2. (Original) The method of Claim 1 wherein the step of loading the decryption keys into the memory is performed without also loading a design into the PLD.

3. (Original) The method of Claim 1 wherein the step of loading the decryption keys into the memory is performed without the use of a device programmer.

4. (Currently Amended) A programmable logic device (PLD) comprising:

a test access port for testing the PLD; and

a circuit for loading at least one decryption key through the test access port.

5. (Original) The PLD of Claim 4 wherein the test access port is a JTAG port.

6. (New) The method of Claim 1, further comprising:

configuring the PLD for a non-secure mode prior to the loading the decryption keys; and

configuring the PLD for a secure mode after the loading the decryption keys.

7. (New) The method of Claim 6, further comprising:

erasing the decryption keys from the memory when configuring the PLD for the non-secure mode.

8. (New) The method of Claim 7, further comprising:

clearing a design from a configuration memory of the PLD when configuring the PLD for the non-secure mode.

9. (New) The method of Claim 1, further comprising:

reading the decryption keys using the JTAG port for verification.

10. (New) The PLD of Claim 4, further comprising:

a decryptor for decrypting an encrypted bitstream using the at least one decryption key.

11. (New) The PLD of Claim 10, further comprising:

a key memory for storing the at least one decryption key.

12. (New) The PLD of Claim 11, further comprising:

programmable logic;

configuration memory coupled to the programmable logic for configuring the programmable logic to perform a desired function; and

configuration logic coupled between the decryptor and the configuration memory for providing programming information to the configuration memory;

wherein the programming information comprises at least a portion of a decrypted bitstream provided by the decryptor.